**HALF ADDER**

**RTL Schematic:**



**Main Program:**

module half(a,b,s,c);

input a,b;

output s,c;

xor(s,a,b);

and(c,a,b);

endmodule

**Test Bench Program:**

module tb;

reg a = 1'b0;

reg b = 1'b0;

wire s;

wire c;

ha UUT (

.a(a),

.b(b),

.s(s),

.c(c));

initial begin

// ------------- Current Time: 200ns

#200;

b = 1'b1;

// -------------------------------------

// ------------- Current Time: 300ns

#100;

a = 1'b1;

b = 1'b0;

// -------------------------------------

// ------------- Current Time: 400ns

#100;

b = 1'b1;

end

endmodule

**Device utilization summary:**

Selected Device : 3s250epq208-4

Number of Slices: 1 out of 2448 0%

Number of 4 input LUTs: 2 out of 4896 0%

Number of IOs: 4

Number of bonded IOBs: 4 out of 158 2%

**Timing Detail:**

Data Path: a to c

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 2 1.218 0.622 a\_IBUF (a\_IBUF)

LUT2:I0->O 1 0.704 0.420 c1 (c\_OBUF)

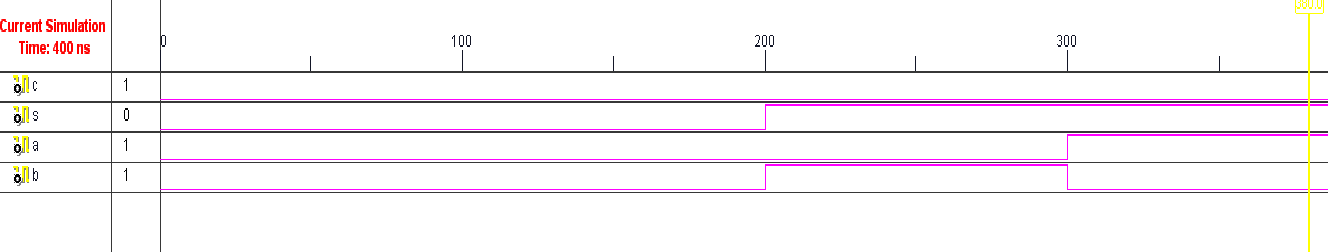
OBUF:I->O 3.272 c\_OBUF (c)

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Total 6.236ns (5.194ns logic, 1.042ns route)

(83.3% logic, 16.7% route)

**Simulation Output:**

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